High Voltage Power Operational Amplifier

FEATURES

- RoHS COMPLIANT
- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION 350V
- LOW QUIESCENT CURRENT TYP. 2.2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT 120mA PEAK

APPLICATIONS

- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER AND DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

DESCRIPTION

The PA441 is a high voltage monolithic MOSFET operational amplifier with improved noise and bandwidth performance compared to similar previous products. Features previously found only in hybrid designs are offered in this monolithic package, with improved reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitation and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA441DF is packaged in a 24 pin PSOP (JEDEC MO-166) package. The metal heat slug of the PA441DF is isolated in excess of full supply voltage.

The PA441DW is packaged in Apex Microtechnolgy's hermetic ceramic PIP package. The alumina ceramic isolates the die in excess of full supply voltage.

The PA443DF has two PA441 dies packaged in a 24 pin PSOP (JEDEC MO-166)package. The heatslug of the PA443DF package is isolated in excess of full supply voltage

FIGURE 1. Equivalent Schematic

(One of 2 Amplifiers for the PA443)

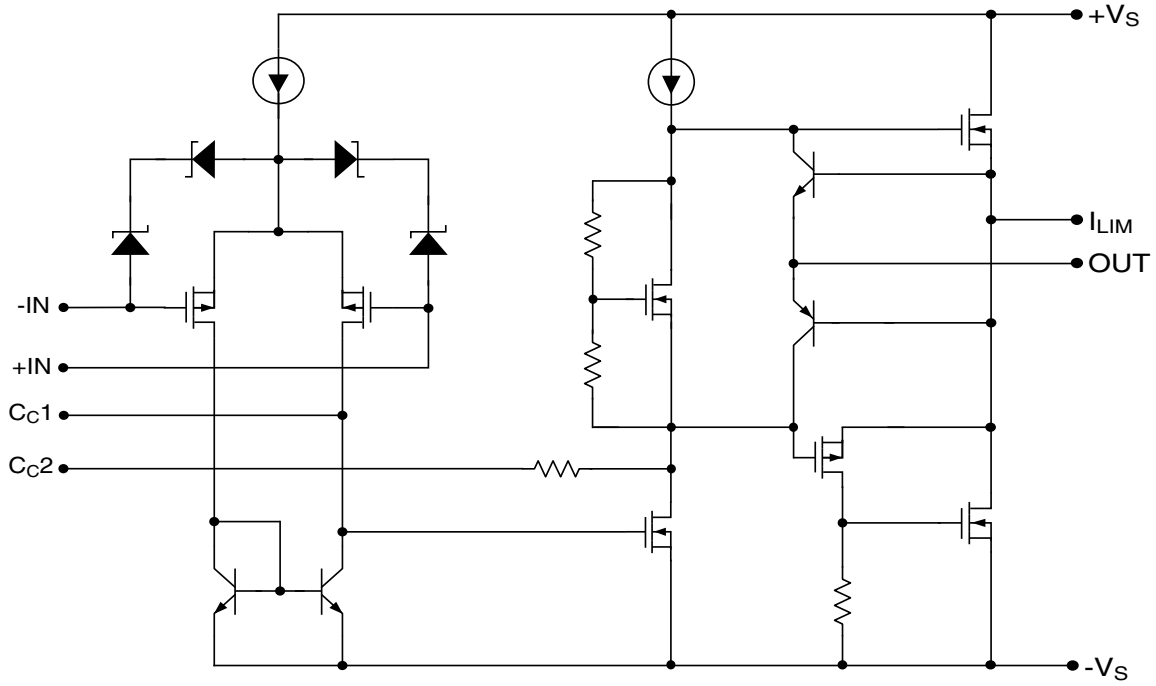
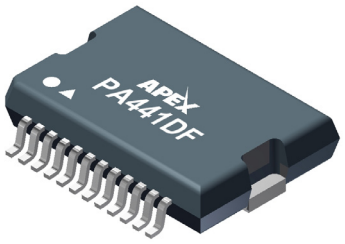
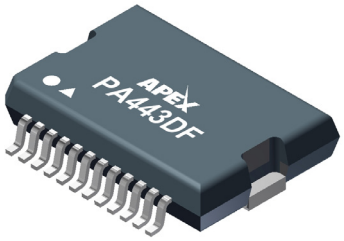


FIGURE 2. Package Style



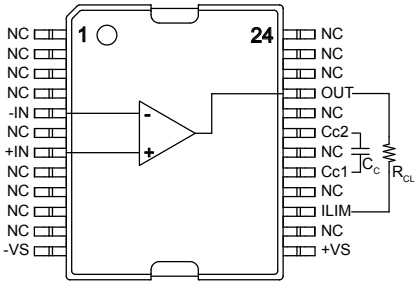
24-PIN PSOP
PACKAGE STYLE DF

10-PIN CERAMIC SIP
PACKAGE STYLE DW

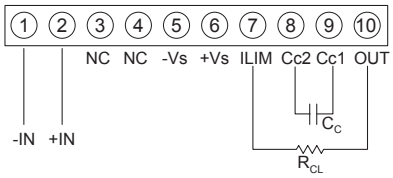


24-PIN PSOP
PACKAGE STYLE DF

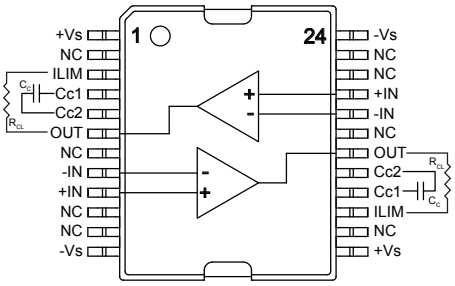
FIGURE 3. External Connections.



PA441DF



PA441DW



PA443DF

FIGURE 4. Pin Table

PA441DF Pin #	PA441DW Pin #	PA443DF Pin #	Name	Description	Rating
5	1	20, 8	-IN	Inverting Input	+/-16V
7	2	21, 9	+IN	Non-Inverting Input	+/-16V
12	5	24, 12	-Vs	Negative Power Supply	+Vs - (-VS) <= 350V
13	6	1, 13	+Vs	Positive Power Supply	+Vs - (-VS) <= 350V
15	7	3, 15	ILIM	Current Limit	n/a
17	9	4, 16	Cc1	Compensation	+Vs - (-VS)
19	8	5, 17	Cc2	Compensation	+Vs - (-VS)
21	10	6, 18	OUT	Output	n/a
1-4, 6, 8-11, 14, 16, 18, 20 22-24	3, 4	2, 7, 10, 11, 14, 19, 22, 23	NC	No Connection	n/a

NOTES: 1. For C_C values, see graph on page 4.
2. C_C must be rated for full supply voltage.

CAUTION The PA441 is constructed from MOSFET transistors. ESD handling procedures must be observed.

1. CHARACTERISTICS AND SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	PA441DF / PA441DW / PA443DF (note 8)		
	Min	Max	Units
SUPPLY VOLTAGE, +Vs to –Vs		350	V
OUTPUT CURRENT, continuous within SOA		60	mA
OUTPUT CURRENT, peak		120	mA
POWER DISSIPATION, continuous @ T_C = 25°C (Note9)		12 / 9 /12	W
INPUT VOLTAGE, differential T_C	-16	+16	V
INPUT VOLTAGE, common mode	-Vs	+Vs	V
TEMPERATURE, pin solder - 10 sec		220	°C
TEMPERATURE, junction (Note 2)		150	°C
TEMPERATURE, storage	-65	150	°C
TEMPERATURE RANGE, powered (case)	-40	125	°C

SPECIFICATIONS

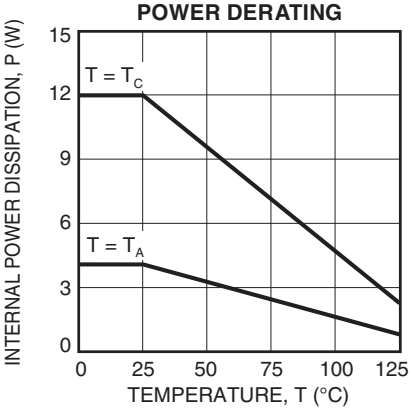
Parameter	Test Conditions (Note 1)	PA441DF / PA441DW / PA443DF (Note 8)			
		Min	Typ	Max	Units
INPUT					
OFFSET VOLTAGE, initial			5	20	mV
OFFSET VOLTAGE, vs. temperature (Note 3)	25° to 85°C		17	250	µV/°C
OFFSET VOLTAGE, vs. temperature (Note 3)	-25° to 25°C		18	500	µV/°C
OFFSET VOLTAGE, vs. supply			3		µV/V
OFFSET VOLTAGE, vs. time			80		µV/kh
BIAS CURRENT, initial (Note 6)			50/100/50	200/200/200	pA
BIAS CURRENT, vs. supply			2		pA/V
OFFSET CURRENT, initial (Note 6)			50/100/50	200/200/200	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			3		pF
COMMON MODE, voltage range		$+V_S$ - 12			V
COMMON MODE, voltage range		$-V_S$ + 12			V
COMMON MODE REJECTION, DC	V_{CM} = ± 90V DC	84	115		dB
NOISE, input referred	20kHz BW, Gain = 2, Cc = 68pF		12		µV RMS
GAIN					
OPEN LOOP at 15Hz	R_L = 5K	90	103		dB
BANDWIDTH, gain bandwidth product	@ 1MHz		10		MHz
POWER BANDWIDTH	280V p-p		35		kHz

Parameter	Test Conditions (Note 1)	PA441DF / PA441DW / PA443DF (Note 8)			
		Min	Typ	Max	Units
OUTPUT					
VOLTAGE SWING	I_O = 40mA	+/-V_S -/+12	+/-V_S -/+10		V
CURRENT, peak (Note 4)		120			mA
CURRENT, continuous		60			mA
SETTLING TIME to 0.1%	10V step, A_V = -10		2		µs
SLEW Rate	C_C = 4.7pF		32		V/µs
RESISTANCE, 10 mA (note 5)	R_{CL} = 0		91		Ω
RESISTANCE, 40 mA (note 5)	R_{CL} = 0		65		Ω
POWER SUPPLY					
VOLTAGE		+/-10	+/-150	+/-175	V
CURRENT, quiescent (note 9)			2.2	2.5	mA
THERMAL					
PA441DF RESISTANCE, AC junction to case	F > 60Hz		6	7	°C/W
PA441DF RESISTANCE, DC junction to case	F < 60Hz		9	11	°C/W
PA441DF RESISTANCE, junction to air (note 6)	Full temperature range		25		°C/W
PA441DW RESISTANCE, AC junction to case	F > 60Hz		7	10	°C/W
PA441DW RESISTANCE, DC junction to case	F < 60Hz		12	14	°C/W
PA441DW RESISTANCE, junction to air (note 6)	Full temperature range		30		°C/W
PA443DF RESISTANCE, AC junction to case, single amplifier	F > 60Hz		6	7	°C/W
PA443DF RESISTANCE, DC junction to case, single amplifier	F < 60Hz		9	11	°C/W
PA443DF RESISTANCE, AC junction to case, both amplifier (note 7)	F > 60Hz		3.3	4	°C/W
PA443DF RESISTANCE, DC junction to case, both amplifier (note 7)	F < 60Hz		5	6	°C/W
PA443DF RESISTANCE, junction to air (note 6)	Full temperature range		25		°C/W
TEMPERATURE RANGE, case	Meets full range spec's	-25		+85	°C

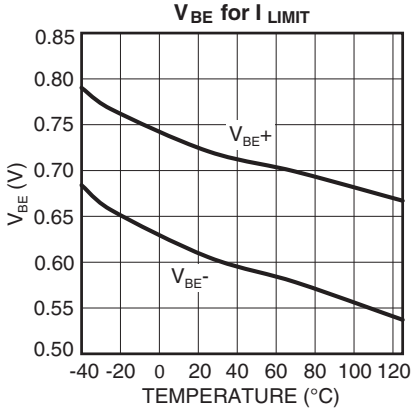
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 6.8pF. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Sample tested by wafer to 95%.
4. Guaranteed but not tested.
5. The selected value of R_{CL} must be added to the values given for total output resistance.
6. Rating applies with solder connection of heatslug to a minimum 1 square inch foil area of the printed circuit board.
7. Rating applies when power dissipation is equal in the two amplifiers.
8. Specifications separated by / indicate values for the PA441DF, PA441DW and PA443DF respectively.
9. Specifications are for individual amplifiers in PA434DF, unless otherwise noted.

2. TYPICAL PERFORMANCE GRAPHS

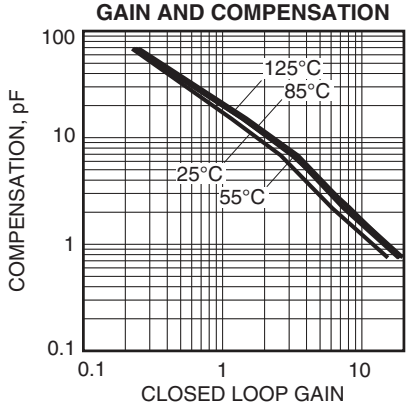
POWER DERATING



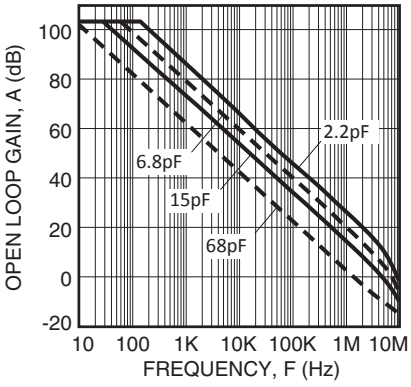
V_{BE} for I_{LIMIT}



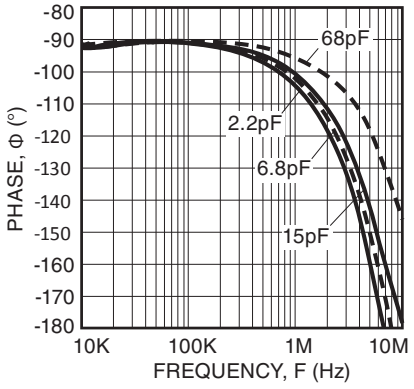
GAIN AND COMPENSATION



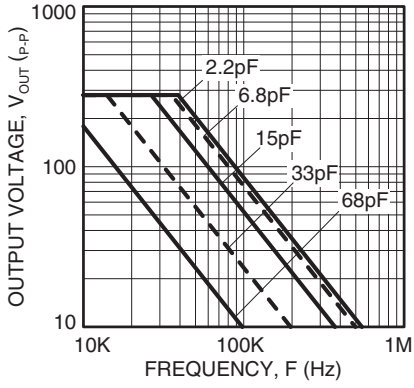
SMALL SIGNAL RESPONSE



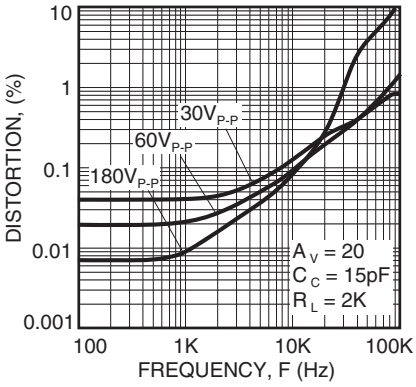
PHASE RESPONSE



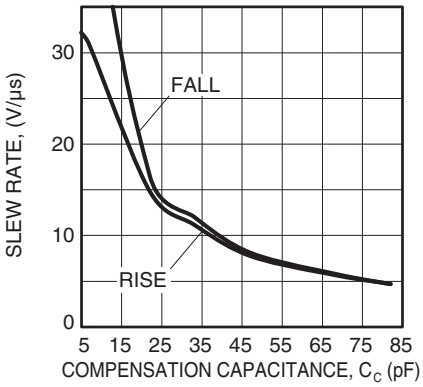
POWER RESPONSE



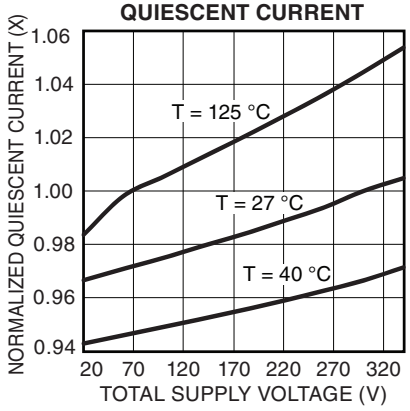
HARMONIC DISTORTION



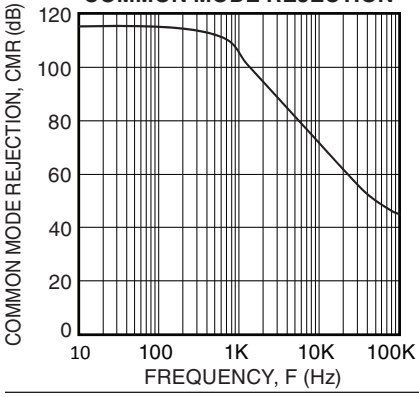
SLEW RATE



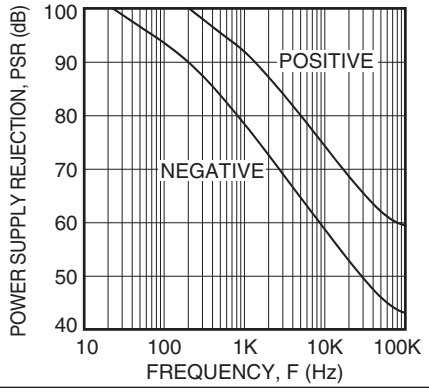
QUIESCENT CURRENT



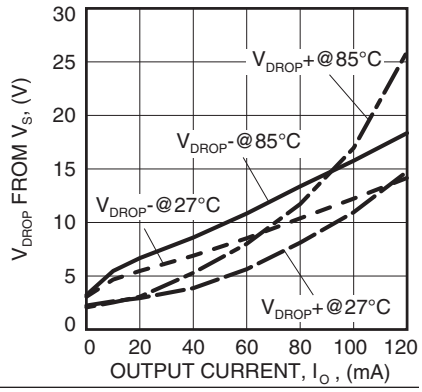
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



TYPICAL APPLICATION

Two PA441 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 volt total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

For further information Application Note 20: "Bridge Mode Operation of Power Amplifiers"

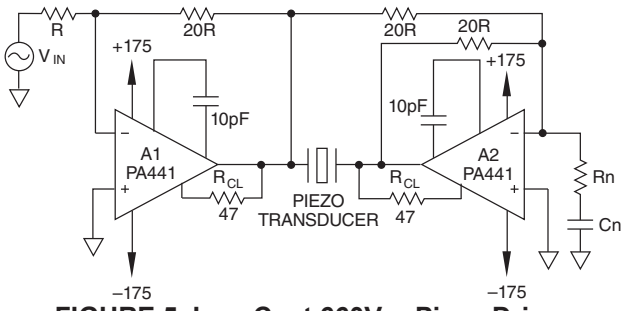


FIGURE 5. Low Cost 660V_{P-P} Piezo Driver

3. APPLICATIONS INFORMATION

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex Microtechnology's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

3.1 PHASE COMPENSATION

Open loop gain and phase shift both increase with increasing temperature. The GAIN AND COMPENSATION typical graph shows closed loop gain and phase compensation capacitor value relationships for four case temperatures. The curves are based on achieving a phase margin of 50°. Calculate the highest case temperature for the application (maximum ambient temperature and highest internal power dissipation) before choosing the compensation. Keep in mind that when working with small values of compensation, parasitics may play a large role in performance of the finished circuit. The compensation capacitor must be rated for at least the total voltage applied to the amplifier and should be a temperature stable type such as NPO or COG. The compensation capacitor value should be as large as possible to avoid possible overshoot issue if there are no input signal clipping circuits.

3.2 OTHER STABILITY CONCERNS

Compensation analysis is supported by 3 plots in the data sheet. These are the “SMALL SIGNAL RESPONSE”, “PHASE COMPENSATION”, and “GAIN AND COMPENSATION” plots. In the “SMALL SIGNAL RESPONSE” plot, the amplifier’s open loop gain is shown for 4 different compensation capacitors. As an example, consider the open loop gain curve for Cc=68 pF. If your application needs a closed loop gain of 10 (20 dB), find the intersection of the horizontal line at 20 dB with the Cc = 68 pF curve. This intersection point, which occurs at about 100 kHz, defines the 3 dB BW (band width) of the amplifier circuit. If you need more BW, the curve with Cc = 15 pF will give you a 3 dB BW of about 500 kHz. Next, go to the PHASE RESPONSE plot. This plot shows that at 500 kHz the phase for Cc = 15 pF is about −95°. So the phase margin is about 85°. Now consider the GAIN and COMPENSATION plot. At a gain of 10 this plot shows that you could get by with a Cc as small as 2 pF. Returning to the SMALL SIGNAL RESPONSE plot, this figure shows that with Cc = 2 pF, the 20 dB closed loop gain now intersects the open loop gain curve at about 2 MHz. The price to pay for this increase in BW is a loss of phase margin, from 85° to 50°, because all of the data in the GAIN AND COMPENSATION plot is for a phase margin of 50°.

In most cases the amplifier output will drive some capacitive load. When this occurs, the open loop curves in the SMALL SIGNAL RESPONSE plot are modified by the appearance of a 2nd pole. In other words, the single pole roll-off which has a -1 slope, will break at some point into a -2 slope roll-off. When this happens, the choice of the 2 pF capacitor will not work and the circuit will oscillate. Stability analysis shows that in a stable circuit, the difference in slope at the intersection point between the open loop gain curve and the closed loop gain curve cannot be −2. So if, at the intersection point, the open loop gain has a −2 slope and the closed loop gain has a slope of 0, the circuit will oscillate. To prevent this, reduce the BW of your circuit by increasing the value of Cc. Larger values of Cc will allow the closed loop gain to intersect the open loop gain before the open loop gain curve breaks into its −2 slope. Use the largest value of Cc that you can, while still maintaining sufficient BW for your application. More advanced techniques of compensation are discussed in AN19 and AN47. For example, these notes discuss “feedback zero” compensation which shows how to stabilize an application circuit whose open loop gain curve has a −2 slope. Please contact Apex Application engineers for more information and support.

3.3 CURRENT LIMIT

For proper operation, the current limiting resistor, R_{CL}, must be connected as shown in Figure 3, "External Connections". The current limit can be predicted as follows:

$$I_{LIMIT} = \frac{V_{BE}}{R_{CL}}$$

The "V_{BE} for I_{LIMIT}" performance graph is used to find V_{BE}. On this graph, the V_{BE}+ and V_{BE}− curves show the voltages across the current limiting resistor at which current limiting is turned on. The V_{BE}+ curve shows these turn-on voltages when the amplifier is sourcing current, and the V_{BE}− curve shows these voltages when the amplifier is sinking current.

The current limit can be thought of as a ceiling or limit for safe operation. For continuous operation it is any value between the desired load current and 60 mA (as long as the curves on the SOA graph are not exceeded, please refer to section 3.4 for information on the SOA graph). As an example, suppose the desired load current for the application is 20 mA. In this case we may set a current limit of 30 mA. Starting with the smaller V_{BE}^- of 0.6 we have:

$$R_{CL} = \frac{0.6}{1.03} = 20\Omega$$

For the larger V_{BE}^+ this R_{CL} resistor will allow for a maximum current of:

$$I_{LIMIT} = \frac{0.7}{20} = 35mA$$

This value is still acceptable because it is less than 60 mA. For the case of continuous load currents, check that the current limit does not exceed 60 mA.

The V_{BE} values used above are approximate and can vary with process. To allow for this possibility the user can reduce the V_{BE} = 0.6 value by 20%. This results in a R_{CL} value of 16 Ω. Using this same R_{CL} value and allowing for a 20% increase in the other V_{BE} , the current limit maximum is 52 mA.

The absolute minimum value of the current limiting resistor is bounded by the largest current and the largest V_{BE} in the application. The largest V_{BE} is determined by the coldest temperature in the application. In general the largest V_{BE} is V_{BE}+ = 0.78, which occurs at T = − 40°C. The largest allowed current occurs in pulsed applications where, from the SOA graph, we can see current pulses of 120 mA. This gives us an absolute minimum R_{CL} value of 0.78/0.12 = 6.5 Ω.

3.4 SAFE OPERATING AREA

The MOSFET output stage of the PA441 is not limited by second breakdown considerations as in bipolar output stages. However there are still three distinct limitations:

1. Voltage withstand capability of the transistors.
2. Current handling capability of the die metallization.
3. Temperature of the output MOSFETs.

These limitations can be seen in the SOA (see Safe Operating Area graphs). Note that each pulse capability line shows a constant power level (unlike second breakdown limitations where power varies with voltage stress). These lines are shown for a case temperature of 25°C and correspond to thermal resistances (See Specification table, Thermal, Max, for thermal resistance of specific package types). Pulse stress levels for other case temperatures can be calculated in the same manner as DC power levels at different temperatures. The output stage is protected against transient flyback by the parasitic diodes of the output stage MOSFET structure. However,for protection against sustained high energy flyback external fast-recovery diodes must be used.

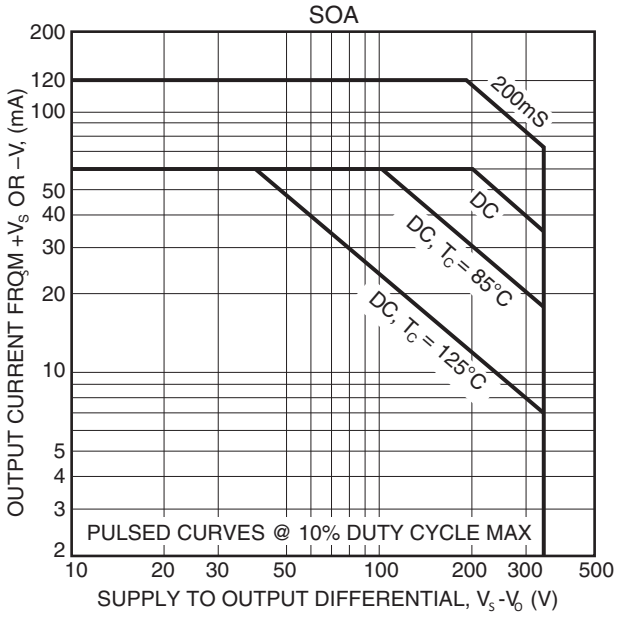
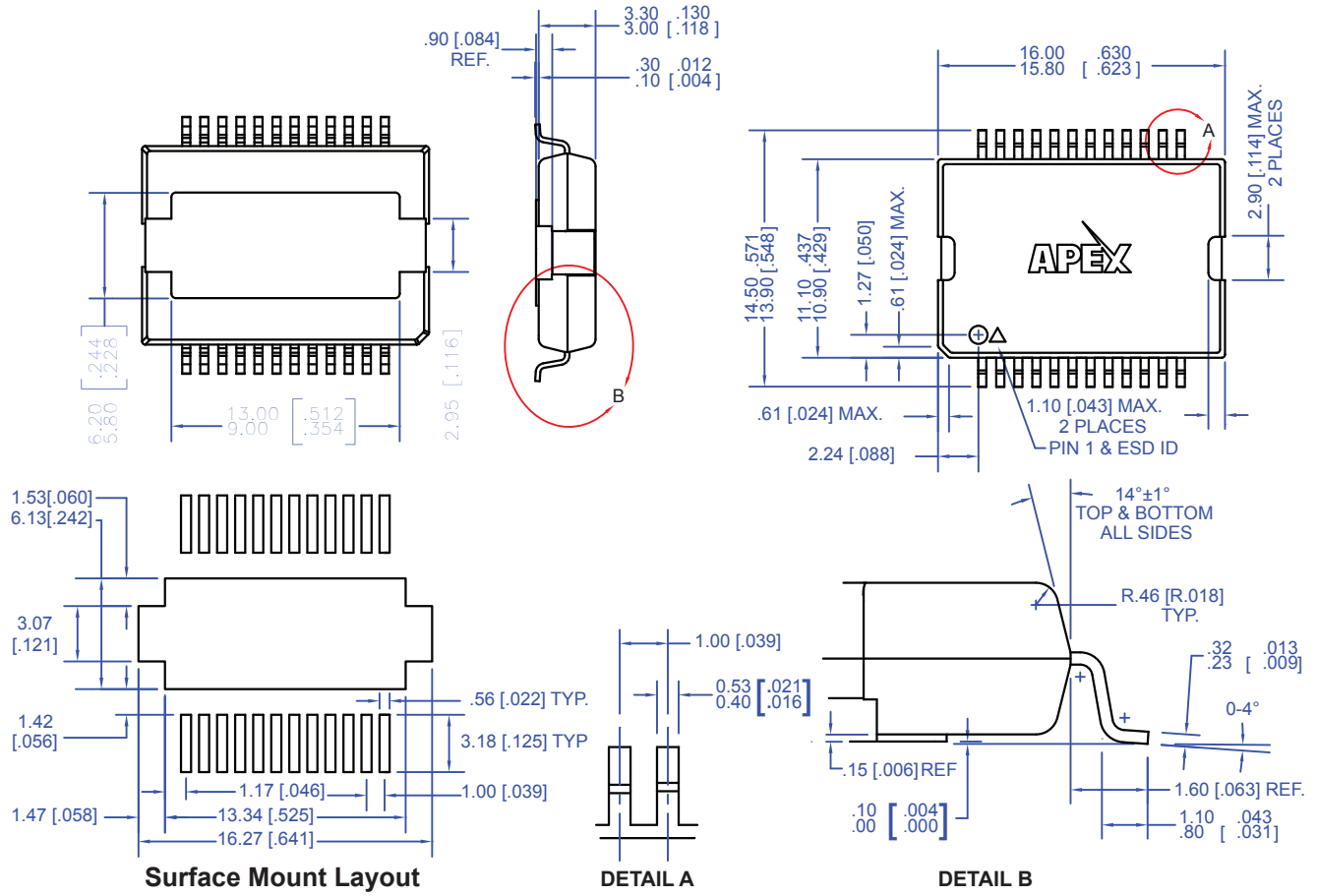


FIGURE 6. Safe Operating Area

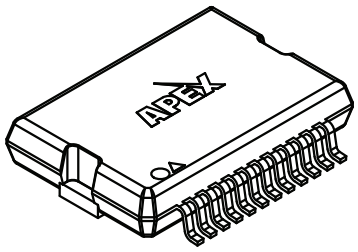


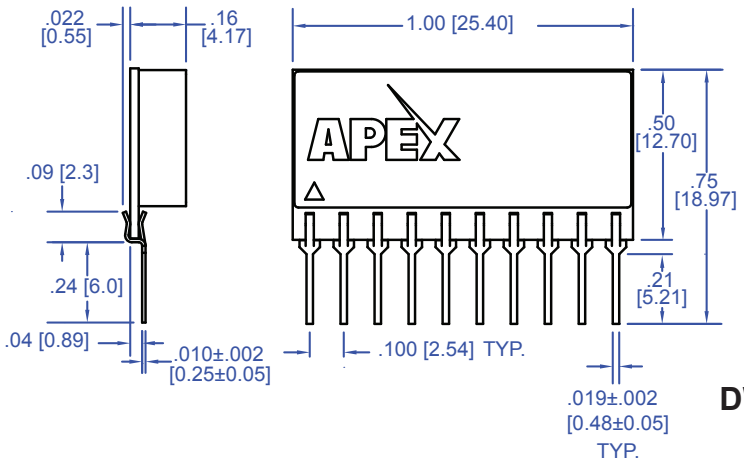
Surface Mount Layout **DETAIL A** **DETAIL B**

NOTES:

1. Dimensions are millimeters & [inches].
2. Bracketed alternate units are for reference only.
3. Dimple on lid & ESD triangle denote pin 1.
4. Pins & Heat Slug: CDA 194 copper with bismuth solder finish
5. Mold compound: MP-8000AN epoxy
6. Package weight: .086 oz. [2.44 g]
7. Suggested surface mount layout for reference only.

DF PACKAGE

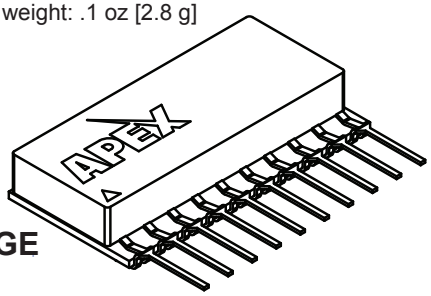




NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Pins: Alloy 510 phosphor bronze plated with matte tin tin (150 - 300µ") over nickel (50 µ" max.) underplate.
4. Package Material: Alumina with hermetic glass seal.
5. Package weight: .1 oz [2.8 g]

DW PACKAGE



3.5 HEATSINKING

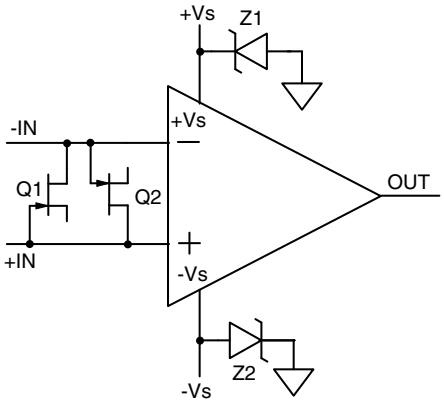
The PA441DF package has a large exposed integrated copper heatslug to which the monolithic amplifier is directly attached. The solder connection of the heatslug to a minimum of 1 square inch foil area on the printed circuit board will result in thermal performance of 25°C/W junction to air rating of the PA441DF. Solder connection to an area of 1 to 2 square inches is recommended. This may be adequate heatsinking but the large number of variables involved suggest temperature measurements be made on the top of the package. Do not allow the temperature to exceed 85°C.

3.6 OVERVOLTAGE PROTECTION

Although the PA441 can withstand differential input voltages up to 16V, in some applications additional external protection may be needed. Differential inputs exceeding 16V will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. For differential sources above 16V, adding series resistance limiting input current to 1mA will prevent damage. Alternatively, 1N4148 signal diodes connected anti-parallel across the input pins is usually sufficient. In more demanding applications where bias current is important, diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 7. In either case the differential input voltage will be clamped to 0.7V. This is sufficient overdrive to produce the maximum power bandwidth.

In the case of inverting circuits where the +IN pin is grounded, the diodes mentioned above will also afford protection from excessive common mode voltage. In the case of non-inverting circuits, clamp diodes from each input to each supply will provide protection. Note that these diodes will have substantial reverse bias voltage under normal operation and diode leakage will produce errors.

FIGURE 7. Overvoltage Protection



Some applications will also need over-voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z_1 and Z_2 in Figure 7.

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